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WAFER MAP ANALYSIS ASSISTING SYSTEM AND WAFER MAP ANALYSIS METHOD

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[There are no amendments to this patent.]

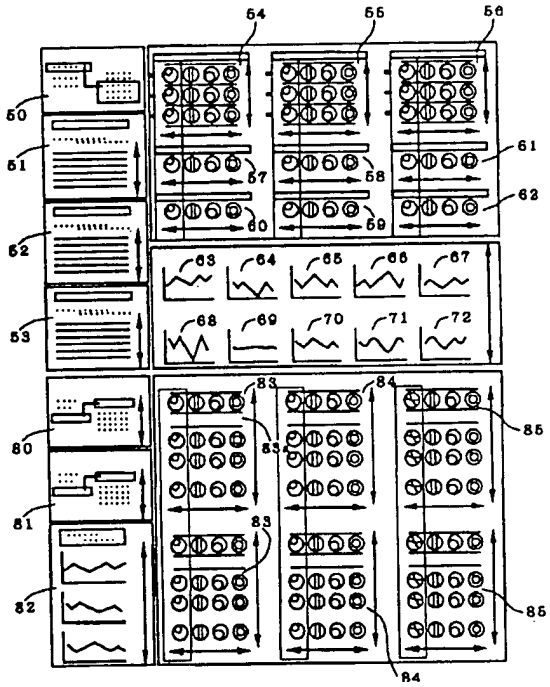
Abstract

Problem

The purpose of this invention is to assist 2-dimensional analysis using a wafer map for solving various problems related to a wafer.

Means to solve

On a screen, the images of the wafer map are displayed with classification for each of the manufacturing steps and items of the device and for inspection. In addition to images of the wafer map, city-related trend charts are also annexed.



Claims

1. A wafer map analysis assisting system characterized by the fact that it has the following means:

an observing means, which forms the map data pertaining to plural wafer maps obtained in the various steps of manufacturing of a semiconductor device and which provides a link indicating the relationship between the map data and said semiconductor manufacturing process;

an input means for inputting text data related to said plural wafer maps, respectively;

a memory means, which stores the prescribed data pertaining to said semiconductor manufacturing process, said map data annexed with said link from said observing means, and said text data from said input means;

and an image display means, which enables display of an image pertaining to said prescribed data concerning said semiconductor manufacturing process and said text data stored in said memory means, and, at the same time, which takes said map data from said memory

means, classifies them according to said link, and enables screen display of the images of wafer maps described in said map data.

2. The wafer map analysis assisting system described in Claim 1 characterized by the fact that said image display means displays the numerical data in said text data as graphs, and, at the same time, it indicates in a visibly identifiable manner the position of the numerical data pertaining to the assigned wafer map on the displayed graph.

3. The wafer map analysis assisting system described in Claim 1 characterized by the fact that said map data contain information of the absolute coordinates and absolute dimensions of various wafer maps, and said image display means makes use of said information of the absolute coordinates and absolute dimensions and displays the images of plural wafer maps overlapped on each other.

4. The wafer map analysis assisting system described in Claim 1 characterized by the fact that said map data contain information of the absolute coordinates and absolute dimensions of various wafer maps, and said image display means makes use of said information of the absolute coordinates and absolute dimensions and displays the image of a wafer map overlapped with an image of mask data.

5. The wafer map analysis assisting system described in Claim 1 characterized by the fact that said map data contain information of the absolute coordinates and absolute dimensions of various wafer maps, and said image display means makes use of said information of the absolute coordinates and absolute dimensions and displays the image of a wafer map overlapped with an image of shape simulation.

6. A wafer map analysis method characterized by the fact that the wafer map analysis method makes use of the image displayed on an image display means to analyze the wafer map, and it has the following steps of operation:

a step in which the map data pertaining to plural wafer maps obtained in the various steps of manufacturing of the semiconductor device are formed and a link indicating the relationship between the map data and said semiconductor manufacturing process is attached to said map data;

a step in which the text data related to said plural wafer maps, respectively, are input;

a step in which the prescribed data pertaining to said semiconductor manufacturing process, said map data annexed with said link from said observing means, and said text data from said input means are stored;

and a step in which in order to analyze said wafer maps, said prescribed data concerning said manufacturing process and said text data stored in said memory means are displayed, and, at the same time, said map data that have been stored are taken and are classified according to said

link, and the images of the wafer maps described in said map data are displayed on said image display means according to the classification.

Detailed explanation of the invention

[0001]

Technical field of the invention

This invention pertains to a wafer map analysis assisting system and wafer map analysis method for analysis of product defects and various abnormalities that occur during the manufacturing process of semiconductor devices by means of images of wafer maps displayed on a monitor.

[0002]

Prior art

On a semiconductor manufacturing line, before treatment of a product lot, a pair wafer or another monitor wafer is used to check the state of various manufacturing devices. When the state of a manufacturing device is checked, mock operation of the manufacturing device is carried out, attachment of dirt on the test wafer is checked, transportation, etc. are checked, and whether or not the manufacturing device is in an appropriate state for manufacturing is checked. After the state checkup, products are manufactured for a prescribed lot number. The numerical data obtained in checking the device state and the numerical data obtained in product treatment are used in quality control of products using a statistical quality control means or the like. Examples of numerical data include the number of dirt particles attached on the wafer, the number of defects formed on the wafer, the dimensions of the pattern formed on the wafer, the thickness of the film formed on the wafer, the measured value of error in mask matching, the concentration of impurities, the resistance of the film formed on the wafer, etc.

[0003]

Also, the map data collected on the manufacturing line are needed if there is doubt in the stability of the operation in statistical quality control (SQC) and if wafer map and chip analysis for a lot have a yield lower than the prescribed level. Usually, the electrical characteristics data obtained after completion of manufacturing and the map data of test results are used to analyze for causes of problems.

[0004]

Figure 7 is a schematic diagram illustrating the constitution of a conventional wafer map analysis assisting system. In Figure 7, (10) represents data concerning the manufacturing

process; (11) represents data pertaining to statistical quality control; (12) represents map data; and (13) represents data pertaining to the analysis of cross-sectional defects. In addition to the manufacturing flow, the data pertaining to the manufacturing process also include numerical data measured in the various manufacturing steps of operation. The manufacturing flow corresponds to the various product manufacturing steps, including the pre-treatment step, film forming step, lithographic step, etching step, defect detecting step, and other steps. The data pertaining to the manufacturing steps are stored as document and computer data, and they can be retrieved appropriately as needed. For example, data (11) pertaining to statistical quality control may be provided for processing into graphic or other easily visible forms. Map data (12) contain data pertaining to the test data adopted in the dummy operation for device control, data pertaining to the wafer extracted as a sample during an actual manufacturing operation, and data obtained in various tests performed after completion of product manufacture. Since map data (12) display various types of information of the image of the wafer, the data amount is large. Data (13) pertaining to analysis of cross-sectional defects are obtained from the image of wafer cross section as observed on a scanning electron microscope. Data (11) pertaining to statistical quality control, map data (12), etc. are provided as the document and computer data.

[0005]

Figure 8 is a schematic diagram illustrating an example of the relationship between the manufacturing process and measurement devices. In Figure 8, steps ST1-ST5 are the pre-treatment step, film forming step, lithographic step, etching step, and defect checking step, respectively. It is also possible to perform dummy operation in the film forming step before beginning the manufacturing operation using a monitor wafer to check for dust. Images (19) of sites where dust is attached on the wafer are collected as map data (19). Dummy operation may also be carried out for other steps of operation.

[0006]

After film forming step ST2, the thickness of the formed film is measured, and map data (20a) are formed. From map data (20a), for example, wafer map (30) or another image is obtained. Similarly, after each of lithographic step ST3, etching step ST4, and defect checking step ST5, the resist pattern and etching pattern are measured, or defects are determined to form map data (21a)-(23a). Using map data (21a)-(23a), it is possible to obtain wafer maps (31)-(33) as images.

[0007]

A conventional wafer map analysis assisting system is limited to special cases, such as determination of problem generation in the manufacturing process, questions regarding the stability of operation, or generation of a lot with a yield that is lower than the prescribed level, after manufacturing, and data (10) pertaining to the manufacturing process, data (11) pertaining to statistical quality control, map data (12), data (13) pertaining to analysis of defects of cross section, etc. are presented individually.

[0008]

Problems to be solved by the invention

With the aforementioned constitution of a conventional wafer map analysis assisting system, only numerical control is carried out, and map data, event data, and other text data are usually not referenced. Consequently, if an abnormality is not displayed as numerical data, the system cannot function well. This is a disadvantage.

[0009]

For example, even when the numerical data of the checking results are identical, if the distribution of the numerical data, which should be random for a normal wafer, is biased, it is quite possible for problems to occur in the near future. However, when only numerical control is performed, it is inappropriate for the analysis to issue a warning regarding the possibility of problems in the future.

[0010]

Also, statistical quality control using numerical data alone cannot perform an analysis that can influence devices inside the wafer. Also, it is impossible to learn the causes of troubles before performing the analysis of defects. Consequently, problems that could be prevented if they were detected during manufacturing process are overlooked, and the problems may occur in the entire lot.

[0011]

The objective of this invention is to solve the aforementioned problems of conventional methods by providing a type of wafer map analysis assisting system characterized by the fact that by means of wafer maps, it is possible to predict the probability of generation of modulation or other problems caused by masks that will occur due to a peculiar trend of the manufacturing device, precursors of problems, and problems during change in the type of production.

[0012]

Means to solve the problems

The first invention provides a wafer map analysis assisting system characterized by the fact that it has the following means: an observing means, which forms map data pertaining to plural wafer maps obtained in the various steps of manufacturing of the semiconductor device and which provides a link indicating the relationship between the map data and said semiconductor manufacturing process; an input means for inputting text data related to said plural wafer maps, respectively; a memory means, which stores prescribed data pertaining to said semiconductor manufacturing process, said map data annexed with said link from said observing means, and said text data from said input means; and an image display means, which enables display of an image pertaining to said prescribed data concerning said semiconductor manufacturing process and said text data stored in said memory means, and, at the same time, which takes said map data from said memory means, classifies them according to said link, and enables screen display of the images of wafer maps described in said map data.

[0013]

The second invention pertains to the wafer map analysis assisting system of the first invention characterized by the fact that said image display means displays the numerical data in said text data as graphs, and, at the same time, it indicates in a visibly identifiable manner the position of the numerical data pertaining to the assigned wafer map on the displayed graph.

[0014]

The third invention pertains to the wafer map analysis assisting system of the first invention characterized by the fact that said map data contain information of the absolute coordinates and absolute dimensions of various wafer maps, and said image display means makes use of said information of the absolute coordinates and absolute dimensions and displays the images of plural wafer maps overlapped on each other.

[0015]

The fourth invention pertains to the wafer map analysis assisting system of the first invention characterized by the fact that said map data contain information of the absolute coordinates and absolute dimensions of various wafer maps, and said image display means makes use of said information of the absolute coordinates and absolute dimensions and displays the image of a wafer map overlapped with an image of mask data.

[0016]

The fifth invention pertains to the wafer map analysis assisting system of the first invention characterized by the fact that said map data contain information of the absolute coordinates and absolute dimensions of various wafer maps, and said image display means makes use of said information of the absolute coordinates and absolute dimensions and displays the image of a wafer map overlapped with an image of shape simulation.

[0017]

The sixth invention provides a wafer map analysis method characterized by the fact that the wafer map analysis method makes use of the image displayed on an image display means to analyze the wafer map, and it has the following steps of operation: a step in which the map data pertaining to plural wafer maps obtained in the various steps of manufacturing of the semiconductor device are formed and a link indicating the relationship between the map data and said semiconductor manufacturing process is attached to said map data; a step in which the text data related to said plural wafer maps, respectively, are input; a step in which the prescribed data pertaining to said semiconductor manufacturing process, said map data annexed with said link from said observing means, and said text data from said input means are stored; and a step in which in order to analyze said wafer maps, said prescribed data concerning said manufacturing process and said text data stored in said memory means are displayed, and, at the same time, said map data that have been stored are taken out and are classified according to said link, and the images of the wafer maps described in said map data are displayed on said image display means according to the classification.

[0018]

Embodiments of the invention

Embodiment 1. Figure 1 is a block diagram illustrating the constitution of the wafer map analysis assisting system in Embodiment 1. In Figure 1, (1) represents an observing means, which forms the map data pertaining to the plural wafer maps obtained in the various steps of the semiconductor manufacturing process and applies a link that indicates the correlation between the semiconductor manufacturing steps and said map data; (2) represents an input means for inputting numerical data related to the plural wafer maps, respectively; (3) represents a memory means for storing data pertaining to the semiconductor manufacturing process, the map data equipped with the link, and the numerical data; and (4) represents an image display means, which enables display of the image pertaining to the data concerning said semiconductor manufacturing process and the numerical data, and, at the same time, which takes said map data

from said memory means, classifies them according to said link, and enables screen display of images of the wafer maps described in said map data.

[0019]

For example, as shown in Figure 8, observing means (1) contains film thickness measurement device (20) and various other measurement devices, defect checking device (23), etc. Usually, these devices individually hold data (20a)-(23a), respectively. However, when the line processing devices, such as film thickness measurement device (20), etc. are connected online to a computer, upon completion of each processing of each device, the processing records, such as the processing start and end dates and times at each device, are used in data collection and processing by means of CGI (Common Gateway Interface), JAVA (registered trademark) manufactured by Sun Microsystems Inc., or other software. The data collected and processed in this way are stored in a data base in memory means (3). The data that should be stored in memory means (3) include the processing start date and time, end date and time, processing operator, process sequence No. for the lot, process name, processing device code, processing recipe, processing parameters, comment notes, processing wafer number, processing results, etc. Among the necessary data, data that are not transmitted from observing means (1) are input to memory means (3) using input means (2). For example, input means (2) may be the terminal of a computer, or the like. As far as the data file form is concerned, any file that can be handled by an HTML generating program, such as CSV, SYLK, etc., may be adopted. Also, there is no limitation on the data update method, which may be periodic, nonperiodic, automatic, semi-automatic, or manual. The aforementioned necessary data stored to memory means (3) are processed into character information or graphics and are displayed on image display means (4). For a graph, data may be displayed for different devices and equipment. Since the necessary data contain the processing start date and time and the processing end date and time of the device at each site, it is possible to plot the data and any processing date pertaining to manufacturing under the assigned conditions. For the graph, when an internet browser is used, the following methods may be adopted: method in which the data are converted to a graph beforehand and the graph is then converted to a file format for use; method in which a plug-in scheme is adopted for the browser itself and the graph obtained from another application is linked; and method in which the JAVA language is used.

[0020]

Also, in order to display the wafer map, when the processing devices of the manufacturing line are connected to the computer online, upon completion of processing of the lot by each processing device, if the obtained image data are bit map or another uncompressed

file, the format is converted to GIF (Graphics Interchange Format), JPEG (Joint Photographic Expert Group), or another compressed image file, and one file is formed for each event or several related files may be combined to form a file to obtain a data base. When the wafer map output device annexed to the processing device does not have a file output function, one may print the data on a sheet of paper, and then scan the print by a scanner so as to form a file that can be displayed on an internet browser.

[0021]

The wafer maps obtained in the wafer process include those for the film thickness of the insulating film, the film thickness of the metal film, the pattern dimensions, the concentration of impurities, the film resistance, the pattern defects, foreign objects, electrical characteristics, etc. The wafer maps obtained upon completion of the wafer process include those for electrical characteristics, test results, etc. The data file formats include GIF, JPEG, and other formats that can be displayed on an internet browser. Also, the data update methods include the periodic method, nonperiodic method, automatic method, semi-automatic method, and manual method. Any of them may be used. The wafer data pertaining to the wafer maps stored in memory means (3) are displayed as images on image display means (4). In this case, in order to clarify the relationship between map data (20a)-(23a) and the semiconductor manufacturing process, observation means (1) attaches the data pertaining to the processing date and time to the file name of the lot as a link.

[0022]

Figure 2 is a schematic diagram illustrating the idea of the constitution of the wafer map analysis assisting system. When this system is realized by an internet browser or when a single application is constructed, data (10) pertaining to the manufacturing process, data (11) pertaining to statistical quality control, map data (12), and data (13) pertaining to analysis of defects of the cross section are stored as data base (14), as shown in Figure 2. For example, map data (12) and data (13) pertaining to analysis of defects of the cross section are transferred from observation means (1) to memory means (3), and they are stored as data base (14) in memory means (3). For example, data (10) pertaining to the manufacturing process and data (11) pertaining to statistical quality control are input from input means (2), and they are stored as data base (14) in memory means (3). Data base (14) is stored in memory means (3) shown in Figure 1. Data base (14) is retrieved by terminal (15). This terminal (15) is contained in image display means (4).

[0023]

Figure 3 illustrates an example of the constitution of a screen of the wafer map analysis assisting system in Embodiment 1. Roughly, the picture shown in Figure 3 can be divided into two regions, namely, an upper data display region concerning devices and a lower data display region concerning equipment information. (50) represents the region displaying information concerning devices. (51)-(53) represent regions for describing information concerning manufacturing processes for three lots selected by region (50), respectively. (54)-(56) represent collections of wafer maps obtained in the manufacturing processes for the three lots, respectively. (57)-(59) represent collections of wafer maps obtained in measurement of electrical characteristics of the three lots, respectively. (60)-(62) represent collections of wafer maps that indicate test results concerning the three lots, respectively. (63)-(72) represent various trend charts.

[0024]

Trend chart (63) pertains to the change in the yield during the prescribed period. Trend charts (64), (67) and (72) pertain to changes in film thickness and dimensions at different sites in the prescribed period. Trend charts (65) and (70) pertain to changes in the resist dimensions of the pattern at different sites in the prescribed period. Trend charts (66) and (67) pertain to changes in the finished dimensions of the pattern at different sites in the prescribed period. Trend chart (68) pertains to changes in the concentration of impurities in the prescribed period. Trend chart (69) pertains to changes in the resistance in the prescribed period.

[0025]

In region (50) that displays information concerning devices, device types, lot No., etc. are described. By selecting the lot No., information related to the lot is described in the upper picture. In regions (51)-(53) pertaining to the manufacturing process, the processing date, sequence No., step name, recipe, parameters, processing results, judgments, etc. are described. In regions (54)-(56), the wafer maps are displayed in three rows and four columns. In this case, different rows correspond to different steps and equipment. Also, other different meanings may be assigned for the different rows. As far as the picture layout is concerned, as shown in Figure 3, for both the longitudinal and lateral layout configurations, the processing results of the same wafer No. are set as a column (or a row), a series of maps for comparison are displayed in any time sequence, and they are arranged to enable understanding of the change in the map over time. Frames (73)-(75) represent wafer maps belonging to the same wafer No. in various lots, respectively. Also, when all of the information cannot be described in the region, the picture can

be scrolled in the direction indicated by the arrow. It is possible to scroll each set of map data on the screen, and it is also possible to scroll using a menu on the operating system of the computer.

[0026]

In the following, an explanation will be provided for the case when the wafer map analysis assisting system is used for analysis of the reasons for low yield. From trend chart (63), the lot with a low yield and a standard lot are extracted. From the lots displayed in region (50), the extracted lots are selected. By performing this selection, wafer maps corresponding to the lots are displayed in, say, regions (54)-(62). Since wafer maps are compared between the lot with a low yield and the standard lot, it becomes easier for one to see bias in the distribution that does not occur in the lot with standard yield. Upon completion of display of wafer maps for a series of lots, abnormal wafer maps are searched, and wafer maps in lots of the same type or of different types having similar patterns of wafer maps are searched.

[0027]

By comparing maps, such as wafer maps that display device information during the manufacturing process, wafer maps that display electrical characteristics, and wafer maps that display test results, for the same device or between different types, it is also possible for the system to function in a manufacturing line for other types with small lots. For example, for a DRAM, the fail bit map may be taken as a wafer map for displaying test results. In Figure 3, (80) represents the region for selecting information related to the manufacturing process; (81) represents the region for selecting equipment; (82) represents the region for displaying trend charts that display data for each piece of equipment; and (83)-(85) represent regions with wafer maps of different equipment set side by side from the upper row downward in a time sequence. In region (80), the manufacturing date of the corresponding device or an assigned period for range assignment is displayed as information related to the manufacturing process. The trend chart displayed in region (82) is for monitoring data for pieces of equipment.

[0028]

Now, a case will be described in which the causes for generation of abnormal wafer maps are hypothesized by means of attached data after wafer map searching by the wafer map analysis assisting system. Irrespective of the lot and equipment information, by assigning the manufacturing date of the corresponding device or the range of the manufacturing period, all of the map data are displayed in time sequence (regions (83)-(85)). The equipment data include the processing history, maintenance history, alarm history, regular dust check, and other text data. In particular, the wafer map for the regular dust check that can be obtained by using a monitor

wafer is displayed together with other text information by means of row (86). Also, similar to the display of the wafer maps on said devices, for the measurement wafers, the wafer maps for the same wafer No. are set side by side such that the history of the wafers can be compared. For regions (83)-(86) shown in Figure 3, each row has the same wafer No.

[0029]

In this way, when an abnormal wafer map is observed during manufacturing or after manufacturing, by collecting information of the manufacturing process on the picture as shown in the lower section of Figure 3, it is possible to specify the cause for generation of the abnormal wafer map and the date and time of the generation.

[0030]

In addition, by searching the overall view of other lots which might have the same problem in the same period by means of the entire processing history from region (80), it is easier to handle the problem, and it is possible to reliably treat lots that might have the problem.

[0031]

As shown in Figure 3, for first region (50), second regions (51)-(53), third regions (54)-(56), fifth regions (57)-(59), sixth regions (60)-(62), seventh regions (63)-(72), eighth region (80), ninth region (81) and tenth regions (83)-(85), the supply source consists of a total of 10 HTML sources, that is, a HTML (Hyper Text Markup Language) source for each region. In each HTML source, for the necessary data, novel data formation/data renewal are performed at the time of data update. When all of the data are sent from a single worldwide web server, all the data including the text and image files are stored on the worldwide web. On the other hand, it is also possible to scatter the worldwide server according to the type of the data. In this case, by checking the directory of the dispersed file, it is possible to link the text and the image file by HTML. Also, any tool may be adopted as the tool for forming HTML. For each picture on Figure 3, the frame function of HTML is used to form the combined HTML, and the desired data browser is completed.

[0032]

In the explanation of Embodiment 1, three lots were compared with one another. However, it is also possible to use the system for analysis of defects of one lot or any number of plural lots. Also, when control is carried out by internet browser, control is performed by HTML. On the other hand, when it is realized by a single application, program is made within the application. Consider an example when data analysis is carried out by selecting only one lot.

Figure 4 illustrates a screen for image display means (3). When the screen shown in Figure 4 is displayed, the operator first selects the type of device from selecting branch (90a) for devices in lot selection region (90). For example, in selection branch (90a), there is a selection branch for type (1) of DRAM or type (11) of SRAM. When lots are displayed on selection branch (90b) by selection of the device, lot selection is carried out. For the selected lot, the collection of wafer maps obtained in the manufacturing process, the corresponding notes (92b), the collection (93b) of wafer maps obtained in measurement of the electrical characteristics, and the collection (94b) that show test results are displayed. For these displays, in the section of selection branches (92a)-(94a) displayed in inline QC map region (92), electrical characteristics region (93) and test results region (94), the object is changed by selecting the processing sequence, the chart No., and the test No. Also, these data are displayed by graphs in inline QC data region (95), electrical characteristics region (96) and test results region (97). The graphs related to the manufacturing process include the graphs of yield, film thickness and dimensions, and resist dimensions. In this case, there is a yield graph together with the electrical characteristics graph and test result graph. The lot for which each wafer map is displayed is displayed by circles on the graph to make it visible. Region (98) for the equipment information has a structure such that the wafer map and event description can change the display of the time sequence by selecting the equipment and the date range.

[0033]

Embodiment 2. Figure 5 illustrates the configuration of the screen of the wafer map analysis assisting system in Embodiment 2. The upper portion of Figure 5 pertains to the numerical data and map data, just as in the display shown in Figure 4. The lower portion of Figure 5 is the display for analysis by synthesis of wafer maps. The lower-portion display also contains mask data and simulation image data in addition to the wafer maps pertaining to synthesis. The wafer maps are displayed in region (100) which displays the original maps for map synthesis as the materials for synthesis. In this case, original maps (101)-(104) displayed in region (100) are wafer maps selected from the various regions in the upper portion. The map formed by synthesis of said original maps (101)-(104) is synthetic map (105).

[0034]

When maps are synthesized, image display means (4) shown in Figure 1 is used. Map data in the upper portion of Figure 5 are selected, and, at the same time, for each wafer map, color setting including transparency is performed so that even when individual wafer maps are overlapped, it is still possible to distinguish the information. Then, original maps (101)-(104) are set on the overall display picture. For original maps (101)-(104), coordinate conversion is

performed so that common coordinates are held by using the absolute coordinates continued from the map data. Also, original maps (101)-(104) have absolute dimensions continued from the map data, and, with the absolute coordinates taken into consideration, the dimensions of the overlapped maps are overlapped reflecting the ratio of actual dimensions. By further selecting the synthesized original maps from original map region (100) for map synthesis, map synthesis is carried out. In synthetic map (105) shown here, the offset [is zero], that is, the various original maps are completely overlapped for display. Consequently, the fact that the original maps are overlapped is easily observed. However, as shown in Figure 6, it is also possible to add offset for display. In this case, the wafer and the image that displays the chip in it become identical to the original map. In region (106) below synthetic map (105), the coordinates, size, classification, etc. of the synthesized original map are displayed. Among the results of synthesis of region (106), list items are selected by the pointer of a mouse or the like, so that the point in synthetic map (105) corresponding to the selected list item flickers.

[0035]

Also, it is possible to enlarge a portion of synthetic map (105) to assist analysis. Map synthesis enlarged figure (107) is an enlarged view of the assigned portion in synthetic map (105). Since original map (101) represents test results, in region (108) that displays the enlarged view of original map (101), the test data at the boundary portion of the enlarged chip are displayed as passed (double circle) and speck cracks (triangle), or by other symbols. In this way, too, original map (101) reflects the absolute dimensions in the configuration of the chip, etc. In region (109) that displays the enlarged view of original map (102), the results of the electrical characteristics at the chip boundary are displayed together with the numerals indicating whether the results are within or outside specifications. For example, "0.2" represents within specifications, while "1.5" represents outside specifications. Original map (102) also reflects the absolute dimensions for configuration of the chip, etc. Since original map (103) shows foreign objects on the product wafer during the manufacturing process, in region (110) that displays the enlarged view of original map (103), the enlarged chip boundary line and foreign objects are displayed. The size of the foreign objects and the size of the wafer are displayed in a correct ratio in consideration of the absolute dimensions. Since original map (104) displays the state of dust on a wafer to check the state of the equipment, in region (111) which displays the enlarged view of original map (104), the enlarged boundary line of the chip and dust attached on the wafer are displayed. The size of the dust and the size of the wafer are displayed at a correct ratio in consideration of the absolute dimensions. Also, it is possible to display the measurement results of original maps (101) and (102) by HTML. The image data are used directly on original maps (103) and (104). However, for the image data at the time of enlargement, display occurs after the

coordinates and size for the maps are made identical. At the time of enlargement, in order to recognize and compare them such that they are visually identical to each other, it is preferred that the same resolution be adopted.

[0036]

In this case, in region (112), the mask data and the wafer maps are overlapped. As shown in Figure 1, image display means (4) forms coordinates shared by both the mask data and the wafer maps. Then, the common coordinates are used to display the mask data at sites corresponding to the coordinates shown in regions (110) and (111), and, at the same time, the enlarged view of foreign objects shown in region (110) and the enlarged view of dust shown in region (111) are overlapped. In overlapped display (113), the first and second layers of the mask data are displayed. By comparing the mask data with the map data on the wafer, the wiring layout beneath the interlayer insulating film and hardly observable during the manufacturing process becomes clear, and, from the relationship between the foreign objects and dust and the wiring layout, it is possible to understand the influence of generation of foreign objects on the chip during the manufacturing process. Display (114) of region (112) indicates which original maps are overlapped. The mask data are input from input means (2) and are stored in memory means (3).

[0037]

Similarly, it is possible to overlap the shape simulator and the map data. If it is possible to specify the coordinates of the wafer, it is possible to convert the coordinates on image display means (3) to a position on the shape simulator, and to align the position on the shape simulator and the coordinates of the wafer. Consequently, if it is possible to specify the coordinates of the wafer, it is possible to display the sites of dust and foreign objects on the shape simulator, and it is possible to check which defects are related to the sites where abnormalities take place. The results of the shape simulation are input from input means (2) and are stored in memory means (3). The relationship between the site on the wafer map and the position on the shape simulator is displayed in region (115). In region (115), the image by the shape simulation is formed at the same image resolution as that of the wafer maps, and it can be displayed in 3-dimensional format with unified coordinates and size.

[0038]

When the aforementioned function is realized by internet browser, the map data, map synthetic data, data of the enlarged view, and the data of the shape simulator are linked by interface using a clickable map or CGI or other intermediate ware. When it is realized by an

internet browser, as shown in Figure 5, the various division pictures are combined by the frame function of HTML to complete the desired data browser. When dedicated application is adopted, the pixel number for which the data in the map synthetic language are overlapped is calculated, and, by setting a certain threshold, it is also possible to calculate automatically the causal relation between layers.

[0039]

In Embodiment 2, explanation was provided for map synthesis obtained from one lot. However, the same map synthesis can also be performed using the map data of any number of plural lots. When plural lots are used, for example, from the similarity of maps in step 1, it is possible to check for a problem in equipment, etc.

[0040]

Also, in Embodiment 2, explanation was provided for the case of map synthesis with color setting on the image of wafer maps. However, it is also possible to perform setting changes on a map synthetic image, vertical movement between layers, etc.

[0041]

Also, in Embodiment 2, wafer maps are used, and, for example, the mask data, shape simulation, and other data are displayed as 2-dimensional or 3-dimensional images to perform data analysis. However, it is also possible to operate the wafer map analysis assisting system without simultaneously using these data.

[0042]

In the explanation of Embodiments 1 and 2, all the data are collected in one screen of one terminal. However, it is also possible to divide the data for display on plural terminals. In this case, the same effects as those of said Embodiments 1 and 2 can be realized.

[0043]

Also, in Embodiments 1 and 2, no explanation was provided for the computer and data for control of various data. It is possible to either collect the data into a single set or to disperse the data to the hardware in plural sets. Each data set can be searched by a single computer through an online means or the like, and it is only necessary that the various data sets be connected to each other.

[0044]

Also, in Embodiments 1 and 2, when the internet browser was used, GIF or JPEG was used for the image data for image display. However, any data format of image data may be adopted as long as the data can be displayed on the browser using a plug-in data conversion tool. In the explanation, the data were constructed in a case with highest analysis efficiency when synthesizing resolution of the wafer maps of all types. However, it is also possible to adopt it in a case in which the resolution of the images of all of the wafer maps is not equal, and their sizes are different from each other.

[0045]

Also, in Embodiments 1 and 2, no description was provided for the link to the map data. It is also possible to provide linkage between SEM image photographs, etc. for the products during the manufacturing process and the steps and trend charts, and linkage between the trend charts and the documents.

[0046]

Effect of the invention

As explained above, with the wafer map analysis assisting system described in Claim 1 and the wafer map analysis method described in Claim 6, it is easy to determine deviations in 2-dimensional data distribution visually by means of wafer maps displayed on an image display means. Consequently, it is possible to perform data analysis midway during the manufacturing process without waiting to the end of the manufacturing process.

[0047]

For the wafer map analysis assisting system described in Claim 2, it is possible to achieve direct visual recognition of the relationship between wafer maps and graphs. Consequently, analysis efficiency can be increased.

[0048]

For the wafer map analysis assisting system described in Claim 3, by overlapping wafer maps over each other, differences in positions of data displayed on the wafer maps can be recognized visually. Consequently, it is possible to realize a visual comparison between wafer maps easily.

[0049]

For the wafer map analysis assisting system described in Claim 4, it is possible to predict sites where the possibility is high for generation of abnormalities on a mask from the overlap between wafer maps and the mask, and it is possible to analyze each layer.

[0050]

For the wafer map analysis assisting system described in Claim 5, it is possible to observe the shape of a site with a high possibility of generation of abnormalities from a device from the results of the shape simulation for the site corresponding to a position of the wafer map, and it is possible to perform analysis of the cross section of device without using an actual image.

Brief description of the figures

Figure 1 is a block diagram illustrating schematically the constitution of the wafer map analysis assisting system in Embodiment 1.

Figure 2 is a schematic diagram illustrating the constitution of the wafer map analysis assisting system in Embodiment 1.

Figure 3 is a drawing illustrating an example of the constitution of the screen of the wafer map analysis assisting system in Embodiment 1.

Figure 4 is drawing illustrating another example of the constitution of the screen of the wafer map analysis assisting system in Embodiment 1.

Figure 5 is a drawing illustrating an example of the constitution of the screen of the wafer map analysis assisting system in Embodiment 2.

Figure 6 is an enlarged diagram illustrating the synthetic map in Figure 5.

Figure 7 is a schematic diagram illustrating the constitution of a conventional wafer map analysis assisting system.

Figure 8 is a schematic diagram illustrating the relationship between the manufacturing process and wafer maps.

Explanation of symbols

1 Observing means
2 Input means
3 Memory means
4 Image display means
14 Data base
15 Terminal

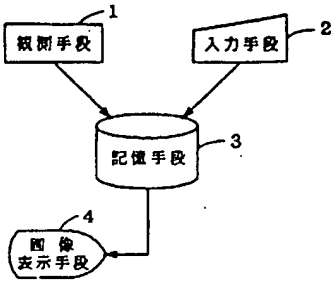


Figure 1

Key: 1 Observing means
2 Input means
3 Memory means
4 Image display means

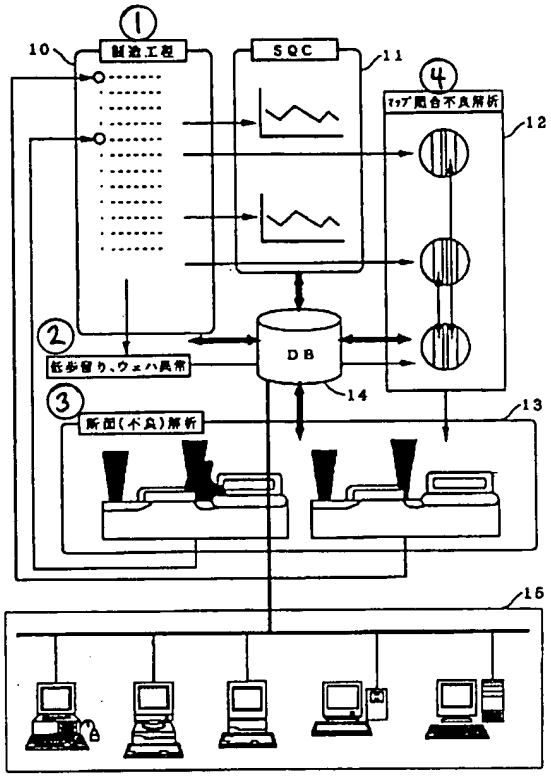


Figure 2

Key: 1 Manufacturing process
2 Low yield and wafer abnormality
3 Analysis of cross section (defects)
4 Analysis of defects in map comparison

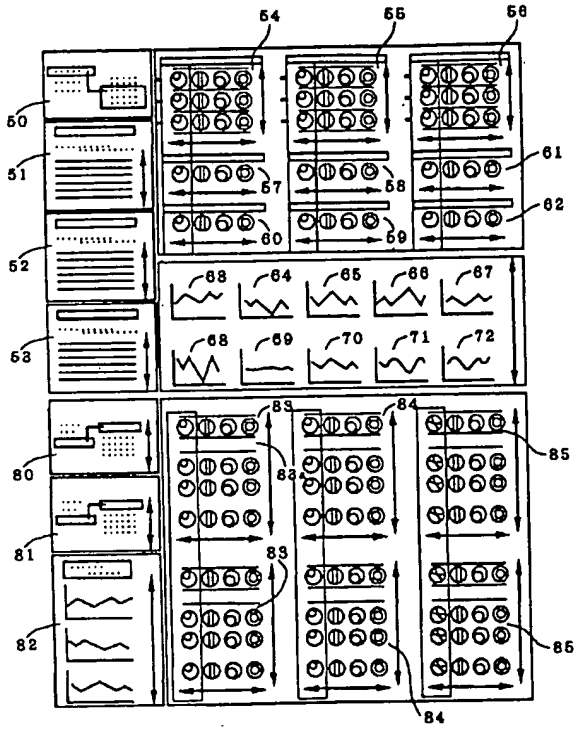

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Figure 3

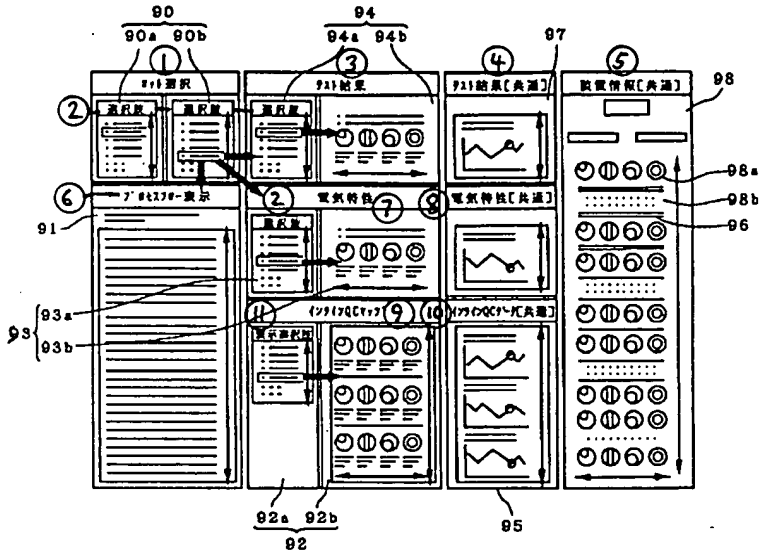

Figure 4

Key:
1 Test selection
2 Selection branch
3 Test results
4 Test results (common)
5 Equipment information (common)
6 Process flow display
7 Electrical characteristics
8 Electrical characteristics (common)
9 Inline QC map
10 Inline QC data (common)
11 Display selection branch

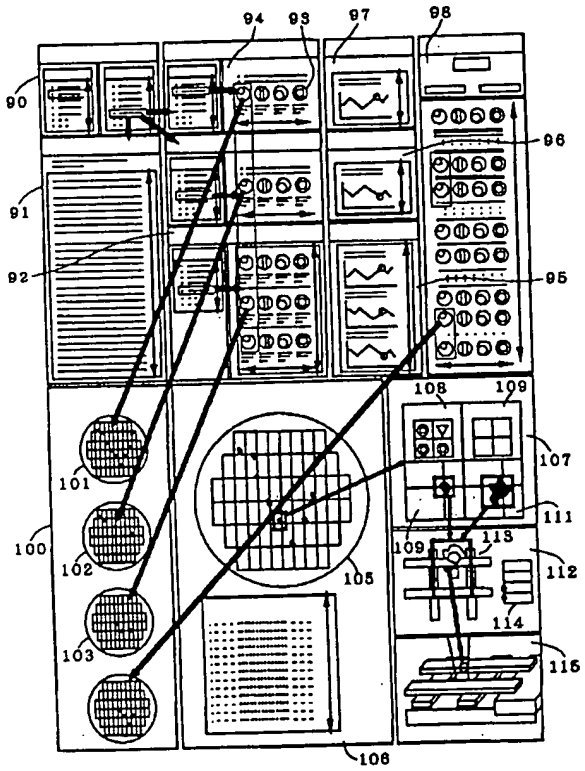
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Figure 5

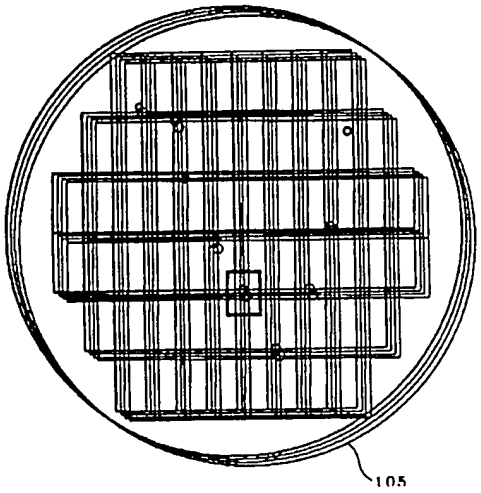

Figure 6

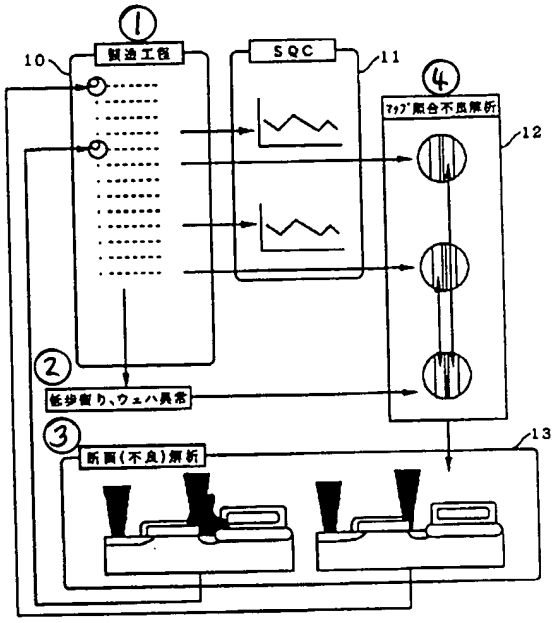

Figure 7

Key: 1 Manufacturing process
2 Low yield and wafer abnormality
3 Analysis of cross section (defects)
4 Analysis of defects in map comparison

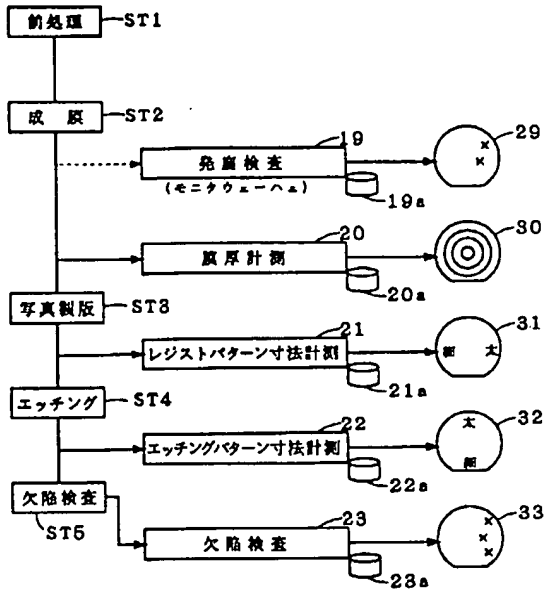

Figure 8

Key:

ST1	Pre-treatment
ST2	Film formation
ST3	Photolithography
ST4	Etching
ST5, 23	Defect check
19	Dust check (monitor wafer)
20	Measurement of film thickness
21	Measurement of resist pattern dimensions
22	Measurement of etching pattern dimensions
31	Fine Wide
32	Wide
	Fine